ACPL-H312 and ACPL-K312

2.5 Amp Output Current IGBT Gate Drive Optocoupler with Low I_{CC} and UVLO in Stretched SO8

Data Sheet

Description

The ACPL-H312/K312 contains a GaAsP LED. The LED is optically coupled to an integrated circuit with a power output stage. These optocouplers are ideally suited for driving power IGBTs and MOSFETs used in motor control inverter applications. The high operating voltage range of the output stage provides the drive voltages required by gate controlled devices. The voltage and current supplied by these optocouplers make them ideally suited for directly driving IGBTs with ratings up to 1200V/100A. For IGBTs with higher ratings, the ACPL-H312/K312 series can be used to drive a discrete power stage which drives the IGBT gate. The ACPL-H312 has an insulation voltage of V_{IORM} = 891 V_{peak} (Option 060). The ACPL-K312 has an issulation voltage of V_{IORM} = 1140 V_{peak} (Option 060).

Application Note

- AN5336 – *Gate Drive Optocoupler Basic Design*

Features

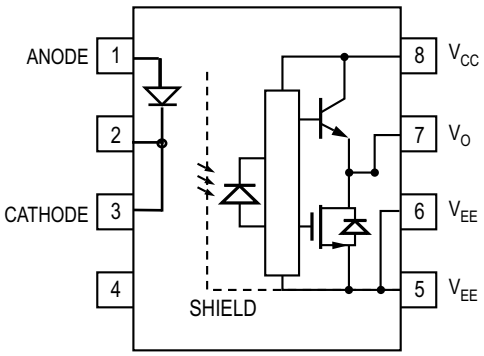
- 2.5 A maximum peak output current
- 2.0 A minimum peak output current
- 15 kV/µs minimum Common Mode Rejection (CMR) at V_{CM} = 1500 V
- 0.5 V maximum low level output voltage (VOL)
- I_{CC} = 3 mA maximum supply current
- Under Voltage Lock-Out protection (UVLO) with hysteresis
- Package Clearance and Creepage at 8mm (ACPL-K312)
- Wide operating VCC range: 15 to 30 Volts
- 500 ns maximum switching speeds
- Industrial temperature range: -40°C to 100°C
- Safety Approval
  - — UL1577 recognized
    3750 Vrms for 1 minute for ACPL-H312
    5000 Vrms for 1 minute for ACPL-K312
  - — CSA Approved
  - — IEC/EN/DIN EN 60747-5-5 Approved
    V_{IORM} = 891 V_{peak} for ACPL-H312
    V_{IORM} = 1140 V_{peak} for ACPL-K312

Applications

- IGBT/MOSFET gate drive
- Inverter for industrial motor
- Inverter for electrical home appliances
- Switching power supplies (SPS)

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD. The components featured in this data sheet are not to be used in military or aerospace applications or environments.

Functional Diagram



NOTE A 1-µF bypass capacitor must be connected between pins V_{CC} and V_{EE}.

Truth Table

LED	$V_{CC} - V_E E$ "POSITIVE GOING" (that is, TURN-ON)	$V_{CC} - V_{EE}$ "NEGATIVE GOING" (that is, TURN-OFF)	V_O
OFF	0–30V	0–30V	LOW
ON	0–11V	0–9.5V	LOW
ON	11–13.5V	9.5–12V	TRANSITION
ON	13.5–30V	12–30V	HIGH

Ordering Information

ACPL-H312/K312 is UL1577 recognized (3750 V_{rms} for 1 minute for ACPL-H312 and 5000 V_{rms} for 1 minute for ACPLK312).

Part Number	Option (RoHS Compliant)	Package	Surface Mount	Tape and Reel	UL 5000 V_{RMS}/ 1 Minute Rating	IEC/EN/DIN EN 60747-5-5	Quantity
ACPL-H312	-000E	Stretched SO-8	X				80 per tube
	-500E		X	X			1000 per reel
	-060E		X			X	80 per tube
	-560E		X	X		X	1000 per reel
ACPL-K312	-000E	Stretched SO-8	X		X		80 per tube
	-500E		X	X	X		1000 per reel
	-060E		X		X	X	80 per tube
	-560E		X	X	X	X	1000 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

ACPL-H312-560E to order product of Stretched SO8 Surface Mount package in Tape and Reel packaging with IEC/EN/ DIN EN 60747-5-5 Safety Approval in RoHS compliant.

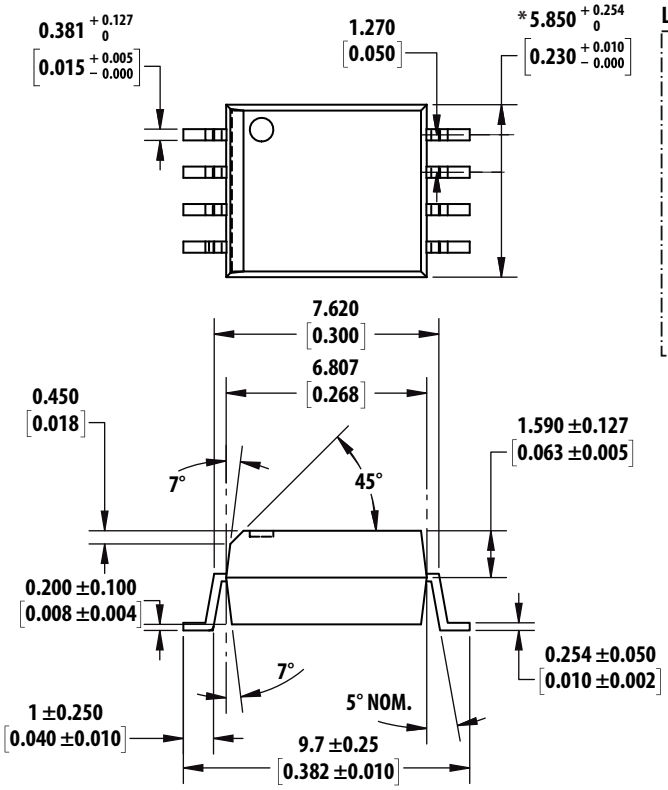
Example 2:

ACPL-H312-000E to order product of Stretched SO8 Surface Mount package in Tube Packaging and RoHS compliant.

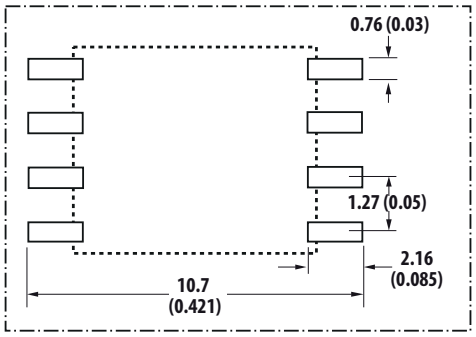
Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

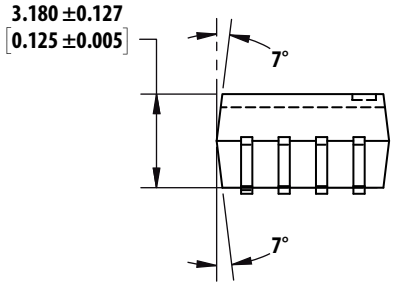
Package Outline Drawings

ACPL-H312 Outline Drawing – Stretched 508



Land Pattern Recommendation

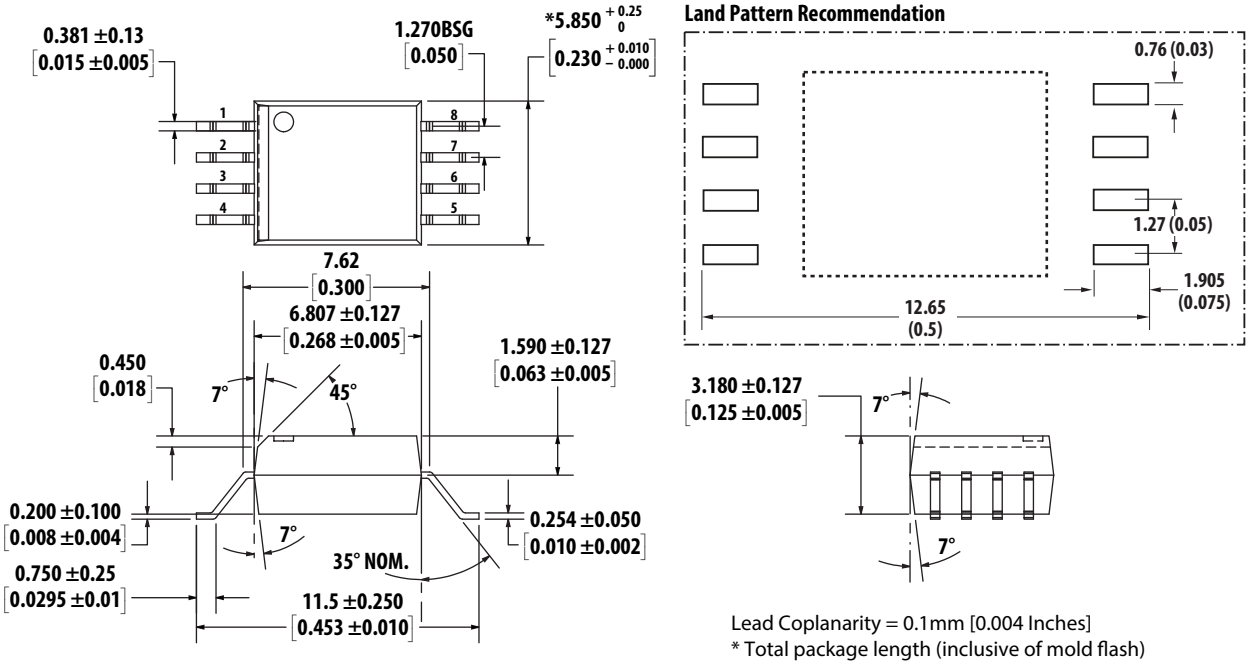




Lead Coplanarity = 0.1mm [0.004 Inches]
* Total package length (inclusive of mold flash)
6.100 ± 0.250 (0.240 ± 0.010)
Floating Lead protusions max. 0.25 [0.0]

Dimensions in Millimeters [Inches]

ACPL-K312 Outline Drawing – Stretched SO8



Lead Coplanarity = 0.1mm [0.004 Inches]
* Total package length (inclusive of mold flash)
6.100 ± 0.250 (0.240 ± 0.010)
Floating Lead protusions max. 0.25 [0.0]

Dimensions in Millimeters [Inches]

Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non- Halide Flux should be used.

Regulatory Information

The ACPL-H342 / ACPL-K342 is approved by the following organizations:

- UL

  Approval under UL 1577, component recognition program up to V_{ISO} = 3750 V_{RMS} for the ACPL-H312 and V_{ISO} = 5000 V_{RMS} for the ACPL-K312), File 55361.
- CSA

  CSA Component Acceptance Notice #5, File CA 88324.
- IEC/EN/DIN EN 60747-5-5 (ACPL-H312/K142 Option 060 Only)

  Maximum Working Insulation Voltage V_{IORM} = 891 V_{peak} (ACPL-H312) and V_{IORM} = 1140 V_{peak} (ACPL-K312).

IEC/EN/DIN EN 60747-5-5 Insulation Characteristics (ACPL-H312/ACPL-K312 Option 060, See Note)

Description	Symbol	ACPL-H312 Option 060	ACPL-K312 Option 060	Units
Installation classification per DIN VDE 0110/39, Table 1f				
or rated mains voltage ≤ 150 V_{rms}		I – IV	I – IV	
for rated mains voltage ≤ 300 V_{rms}		I – IV	I – IV	
for rated mains voltage ≤ 450 V_{rms}		I – III	I – IV	
for rated mains voltage ≤ 600 V_{rms}		I – III	I – IV	
for rated mains voltage ≤ 1000 V_{rms}			I – III	
Climatic Classification		55/100/21	55/100/21	
Pollution Degree (DIN VDE 0110/1.89)		2	2	
Maximum Working Insulation Voltage	V_{IORM}	891	1140	V_{peak}
Input to Output Test Voltage, Method b[a] $V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test with t_m=1s, Partial discharge < 5 pC	V_{PR}	1670	2137	V_{peak}
Input to Output Test Voltage, Method a[a] $V_{IORM} \times 1.6 = V_{PR}$, Type and Sample Test, t_m=10s, Partial discharge < 5 pC	V_{PR}	1426	1824	V_{peak}
Highest Allowable Overvoltage[a] (Transient Overvoltage t_{ini} = 60s)	V_{IOTM}	6000	8000	V_{peak}
Safety-limiting values – maximum values allowed in the event of a failure				
Case Temperature	T_S	175	175	°C
Input Current	$I_{S, INPUT}$	230	230	mA
Output Power	$P_{S, OUTPUT}$	600	600	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$>10^9$	$>10^9$	Ω

a. Refer to IEC/EN/DIN EN 60747-5-5 Optoisolator Safety Standard section of the *Broadcom Regulatory Guide to Isolation Circuits*, AV02-2041EN, for a detailed description of Method a and Method b partial discharge test profiles.

NOTE These optocouplers are suitable for "safe electrical isolation" only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits. Surface mount classification is Class A in accordance with CECC 00802.

Insulation and Safety Related Specifications

Parameter	Symbol	ACPL-H342	ACPL-K342	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	7.0	8.0	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	8.0	8.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.08	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	> 175	> 175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

NOTE All Broadcom data sheets report the creepage and clearance inherent to the optocoupler component itself. These dimensions are needed as a starting point for the equipment designer when determining the circuit insulation requirements. However, once mounted on a printed circuit board, minimum creepage and clearance requirements must be met as specified for individual equipment standards. For creepage, the shortest distance path along the surface of a printed circuit board between the solder fillets of the input and output leads must be considered (the recommended land pattern does not necessarily meet the minimum creepage of the device). There are recommended techniques such as grooves and ribs which may be used on a printed circuit board to achieve desired creepage and clearances. Creepage and clearance distances will also change depending on factors such as pollution degree and insulation level.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	–55	125	°C	
Operating Temperature	T_A	–40	105	°C	
Junction Temperature	T_J	—	125	°C	
Average Input Current	$I_{F(AVG)}$	—	25	mA	a
Peak Transient Input Current (<1-ms pulse width, 300 pps)	$I_{F(TRAN)}$	—	1.0	A	
Reverse Input Voltage	V_R	—	5	V	
"High" Peak Output Current	$I_{OH(PEAK)}$	—	2.5	A	b
"Low" Peak Output Current	$I_{OL(PEAK)}$	—	2.5	A	b
Supply Voltage	$(V_{CC} – V_{EE})$	0	35	V	
Input Current (Rise/Fall Time)	$t_{r(IN)} / t_{f(IN)}$	—	500	ns	
Output Voltage	$V_{O(PEAK)}$	–0.5	V_{CC}	V	
Output Power Dissipation	P_O	—	250	mW	c
Total Power Dissipation	P_T	—	295	mW	d
Lead Solder Temperature	260°C for 10s, 1.6 mm below seating plane				
Solder Reflow Temperature Profile	See Package Outline Drawings				

a. Derate linearly above 70°C free-air temperature at a rate of 0.3 mA/°C.

b. Maximum pulse width = 10 µs.

c. Derate linearly above 78°C free-air temperature at a rate of 5.7 mW/°C.

d. Derate linearly above 78°C free-air temperature at a rate of 6.0 mW/°C. The maximum LED junction temperature should not exceed 125°C.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Note
Power Supply	$V_{CC} – V_{EE}$	15	30	V	
Input Current (ON)	$I_{F(ON)}$	7	16	mA	
Input Voltage (OFF)	$V_{F(OFF)}$	–3.6	0.8	V	
Operating Temperature	T_A	–40	100	°C	

Electrical Specifications (DC)

Unless otherwise noted, all typical values are at T_A = –40°C to 100°C, $I_{F(ON)}$ = 7 mA to 16 mA, $V_{F(OFF)}$ = –3.6V to 0.8V, V_{CC} = 15V to 30V, V_{EE} = Ground) unless otherwise specified. All typical values at T_A = 25°C and $V_{CC} - V_{EE}$ = 30V, unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
High Level Peak Output Current	I_{OH}	0.5	1.5	—	A	$V_O = V_{CC} - 4V$	2, 3, 17	a
		2	—	—	A	$V_O = V_{CC} - 15V$		b
Low Level Peak Output Current	I_{OL}	0.5	2.0	—	A	$V_O = V_{EE} + 2.5V$	5, 6, 18	a
		2	—	—	A	$V_O = V_{EE} + 15V$		b
High Level Output Voltage	V_{OH}	$V_{CC} - 4$	$V_{CC} - 3$	—	V	I_O = –100 mA	1, 3, 19	c, d
Low Level Output Voltage	V_{OL}	—	0.1	0.5	V	I_O = 100 mA	4, 6, 20	
High Level Supply Current	I_{CCH}	—	1.8	3.0	mA	Output open, I_F = 7 mA to 16 mA,	7, 8	
Low Level Supply Current	I_{CCL}	—	1.8	3.0	mA	Output open, V_F = –3.6V to +0.8V	7, 8	
Threshold Input Current Low to High	I_{FLH}	—	2.3	5	mA	I_O = 0 mA, V_O > 5V	9, 15, 21	
Threshold Input Voltage High to Low	V_{FHL}	0.8	—	—	V	I_O = 0 mA, V_O > 5V		
Input Forward Voltage	V_F	1.2	1.5	1.8	V	I_F = 10 mA	16	
Temperature Coefficient of Input Forward Voltage	$\Delta V_F/\Delta T_A$	—	–1.6	—	mV/°C	I_F = 10 mA		
Input Reverse Breakdown Voltage	BV_R	5	—	—	V	I_R = 100 µA		
Input Capacitance	C_{IN}	—	60	—	pF	f = 1 MHz, V_F = 0 V		
UVLO Threshold	V_{UVLO+}	11.0	12.3	13.5	V	V_O > 5V, I_F = 10 mA	22	
	V_{UVLO-}	9.5	11.0	12.0	V	V_O > 5V, I_F = 10 mA	22	
UVLO Hysteresis	$UVLO_{HYS}$	—	1.4	—	V	V_O > 5V, I_F = 10 mA		

a. Maximum pulse width = 50 µs.

b. Maximum pulse width = 10 µs.

c. In this test, V_{OH} is measured with a DC load current. When driving capacitive loads, V_{OH} will approach V_{CC} as I_{OH} approaches 0 amps.

d. Maximum pulse width = 1 ms.

Switching Specifications (AC)

Over recommended operating conditions (T_A = –40°C to 100°C, $I_{F(ON)}$ = 7 mA to 16 mA, $V_{F(OFF)}$ = –3.6V to 0.8V, V_{CC} = 15V to 30V, V_{EE} = Ground) unless otherwise specified. All typical values at T_A = 25°C and $V_{CC} - V_{EE}$ = 30V, unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to High Output Level	t_{PLH}	0.05	0.28	0.5	µs	Rg = 10 Ω, Cg = 10 nF, f = 10 kHz , Duty Cycle = 50%,	12, 13, 14, 23	a
Propagation Delay Time to Low Output Level	t_{PHL}	0.05	0.26	0.5	µs			
Pulse Width Distortion	PWD	—	—	0.3	µs			
Propagation Delay Difference Between Any Two Parts or Channels	PDD ($t_{PHL} - t_{PLH}$)	–0.35	—	0.35	µs			b
Rise Time	t_R	—	0.05	—	µs		23	c
Fall Time	t_F	—	0.05	—	µs			
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	15	30	—	kV/µs	T_A = 25 °C, I_F = 10 mA, to 16 mA, V_{CC} = 30V, V_{CM} = 1500 V	24	d, e
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	15	30	—	kV/µs	T_A = 25 °C, V_F = 0V, V_{CC} = 30V, V_{CM} = 1500V	24	d, f

a. This load condition approximates the gate load of a 1200V/150A IGBT.

b. Pulse Width Distortion (PWD) is defined as $|t_{PHL} - t_{PLH}|$ for any given device.

c. The diff erence between t_{PHL} and t_{PLH} between any two ACPL-H312/K312 parts under the same test condition.

d. Pins 3 and 4 need to be connected to LED common.

e. Common mode transient immunity in the high state is the maximum tolerable dV_{CM}/dt of the common mode pulse, $V_{CM,}$ to assure that the output will remain in the high state (that is, V_O > 15.0V).

f. Common mode transient immunity in a low state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a low state (that is, V_O < 1.0V).

Package Characteristics

Over recommended temperature (T_A = –40°C to 100°C) unless otherwise specifi ed. All typicals at T_A = 25°C.

Parameter	Symbol	Device	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Input-Output Momentary Withstand Voltage[a]	V_{ISO}	ACPL-H312	3750	—	—	V_{RMS}	RH < 50%, t = 1 min., T_A = 25°C		b, c
		ACPL-K312	5000	—	—				c, d
Resistance (Input-Output)	R_{I-O}		—	10^{12}	—	Ω	V_{I-O} = 500 V		c
Capacitance (Input-Output)	C_{I-O}		—	0.6	—	pF	Freq =1 MHz		

a. The input-output momentary withstand voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating, refer to your equipment level safety specification or Broadcom Application Note 1074, *Optocoupler Input-Output Endurance Voltage*.

b. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 4500 Vrms for 1 second leakage detection current limit, I_{I-O} ≤ 5 µA).

c. Device considered a two-terminal device: pins 1, 2, 3, and 4 shorted together and pins 5, 6, 7, and 8 shorted together.

d. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 Vrms for 1 second (leakage detection current limit, I_{I-O} ≤ 5A).

Figure 1 V_{OH} vs. Temperature

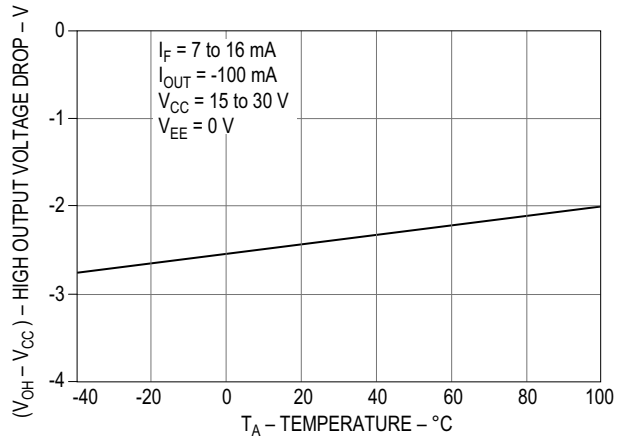


Figure 2 I_{OH} vs. Temperature

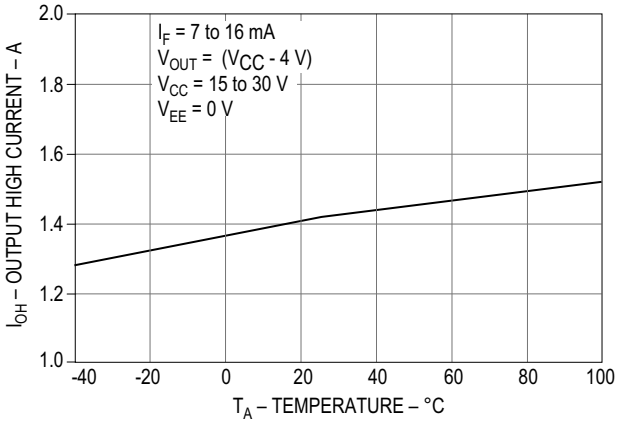


Figure 3 V_{OH} vs. I_{OH}

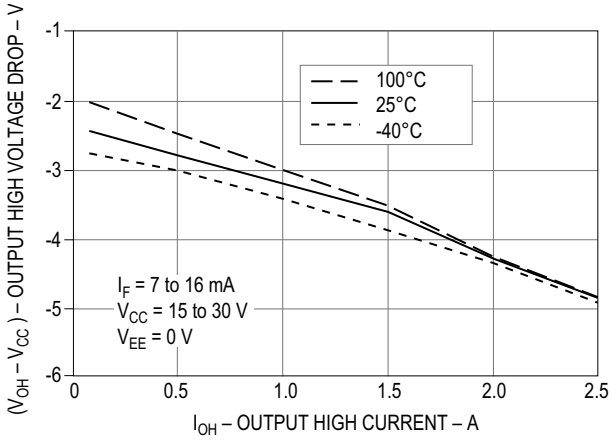


Figure 4 V_{OL} vs. Temperature

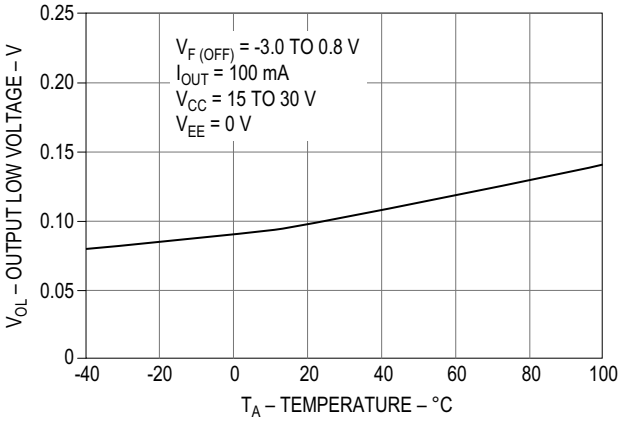


Figure 5 I_{OL} vs. Temperature

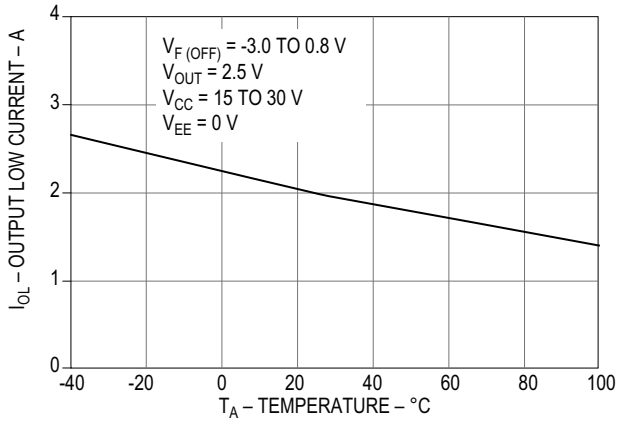


Figure 6 V_{OL} vs. I_{OL}

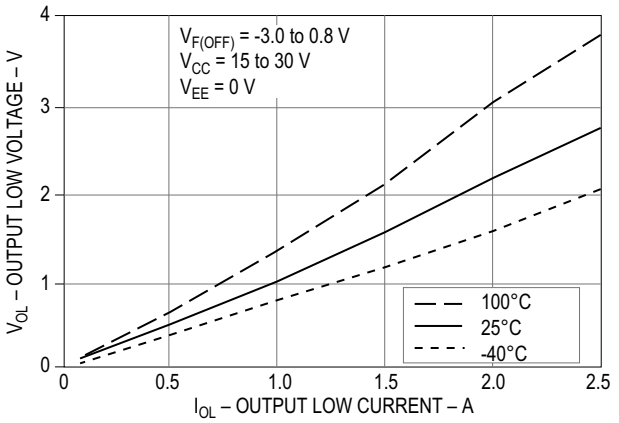


Figure 7 I_{CC} vs. Temperature

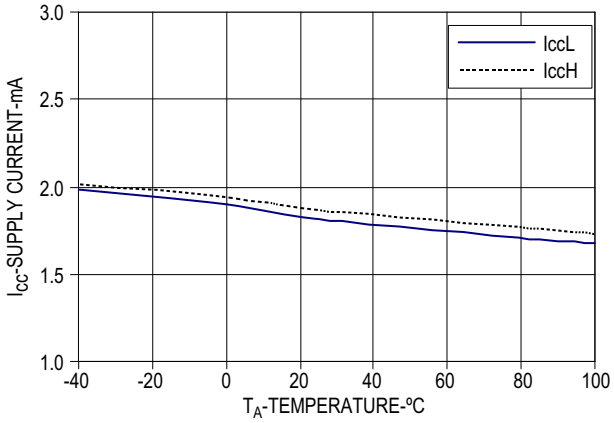


Figure 8 I_{CC} vs. V_{CC}

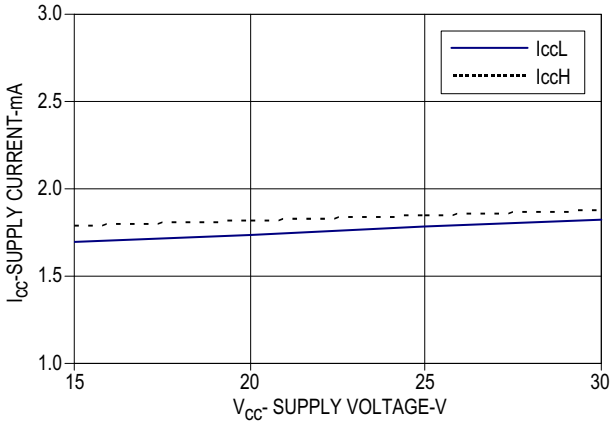


Figure 9 I_{FLH} vs. Temperature

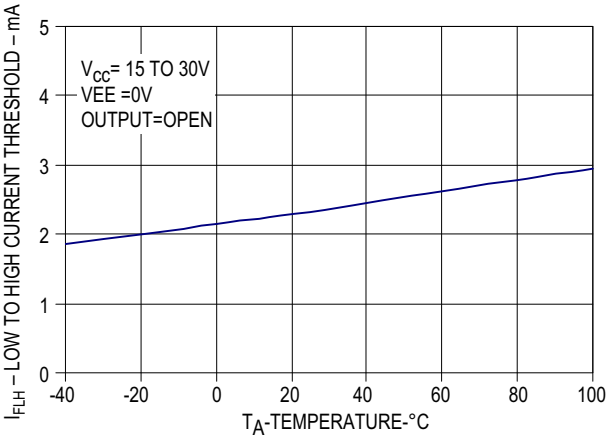


Figure 10 Propagation Delay vs. V_{CC}

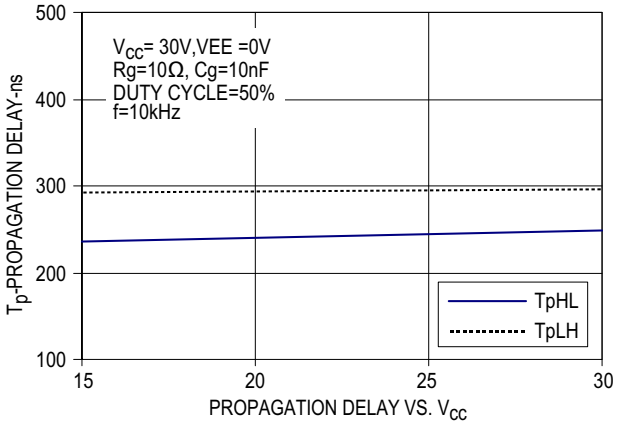


Figure 11 Propagation Delay vs. I_F

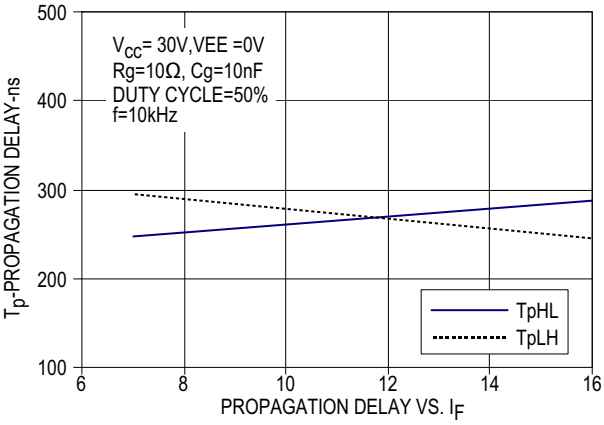


Figure 12 Propagation Delay vs. Temperature

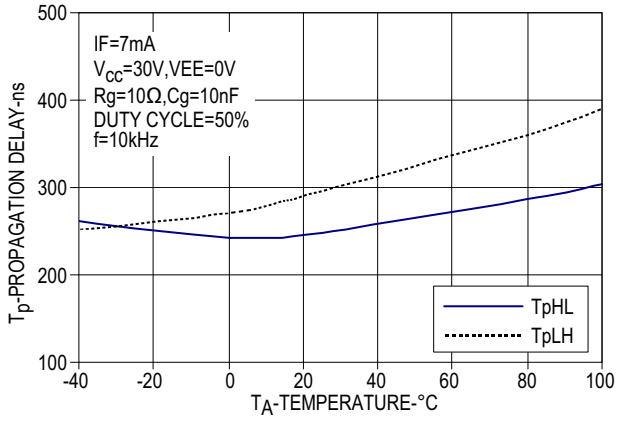


Figure 13 Propagation Delay vs. Rg

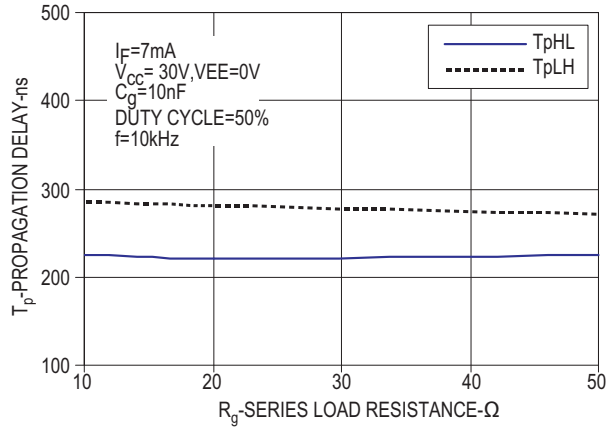


Figure 14 Propagation Delay vs. Cg

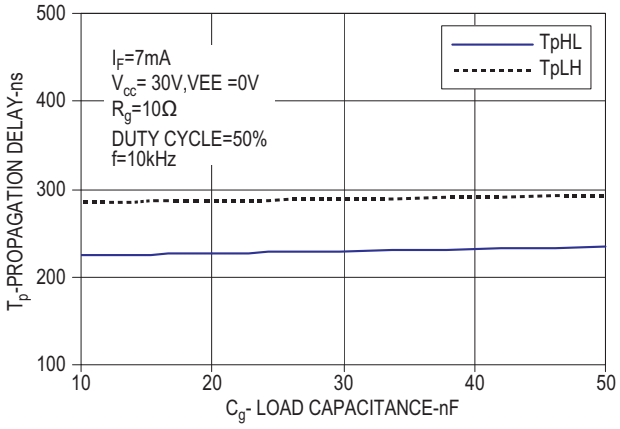


Figure 15 Transfer Characteristics

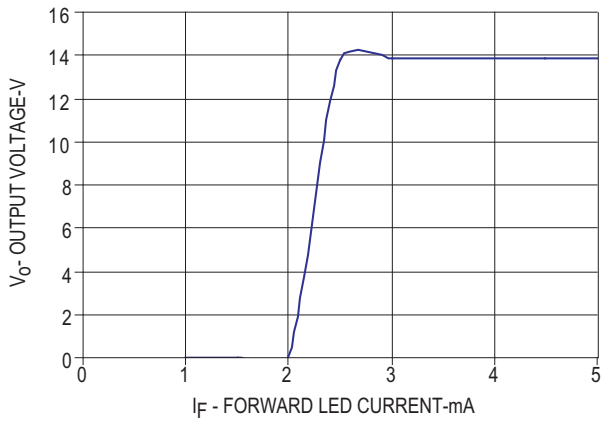


Figure 16 Input Current vs. Forward Voltage

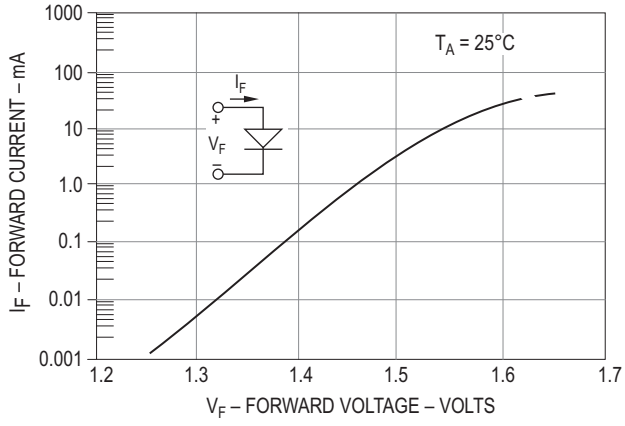


Figure 17 I_{OH} Test Circuit

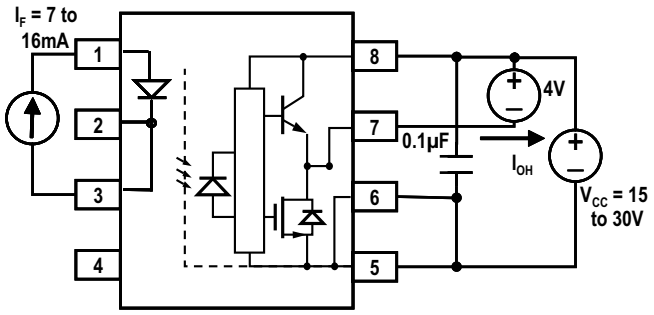


Figure 18 I_{OL} Test Circuit

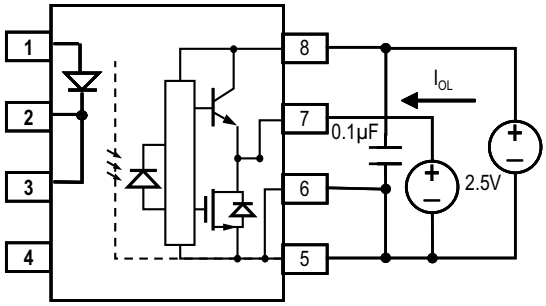


Figure 19 V_{OH} Test Circuit

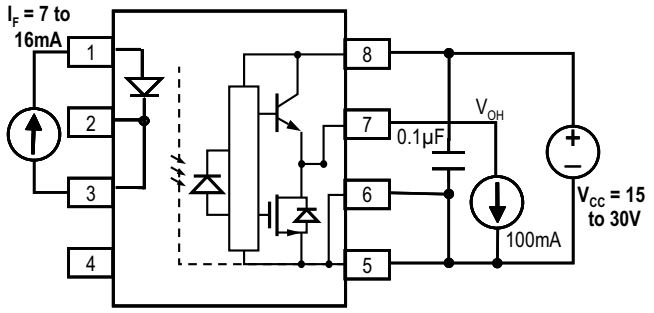


Figure 20 V_{OL} Test Circuit

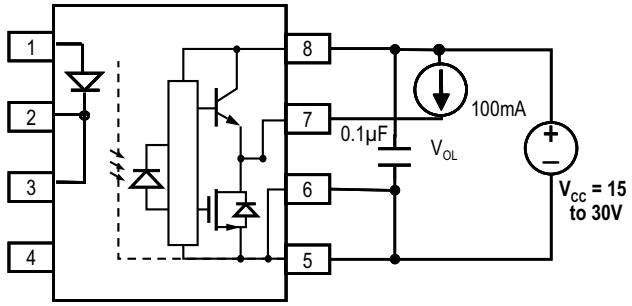


Figure 21 I_{FLH} Test Circuit

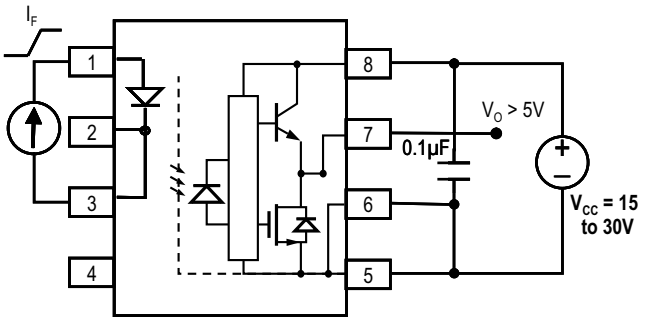


Figure 22 UVLO Test Circuit

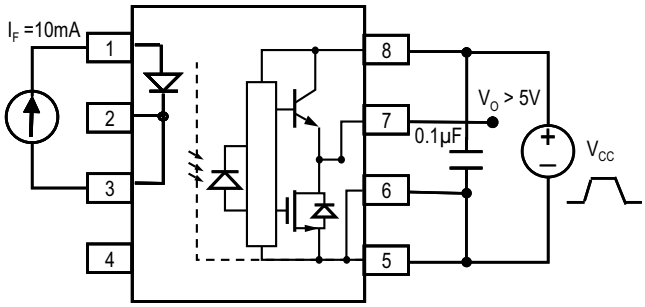


Figure 23 T_{PLH}, tP_{HL}, tr, and tf Test Circuit and Waveforms

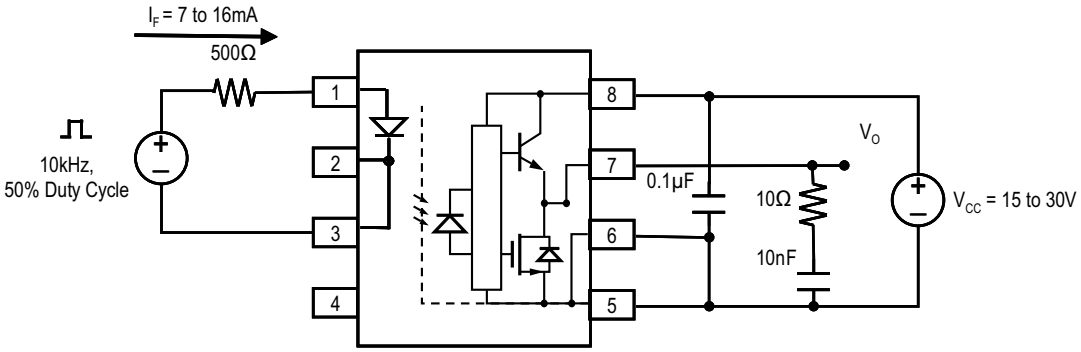
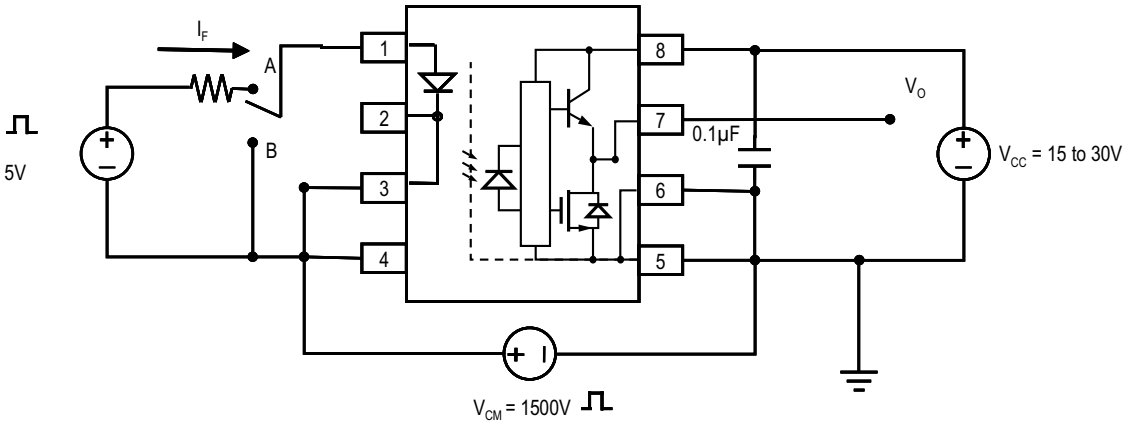


Figure 24 CMR Test Circuit and Waveforms



Typical Application Circuit

Figure 25 and Figure 26 show two gate driver application circuits using ACPL-H312/K312. Application Note AN5336 describes general method on gate drive optocoupler design.

Figure 25 Recommended LED Drive and Application Circuit

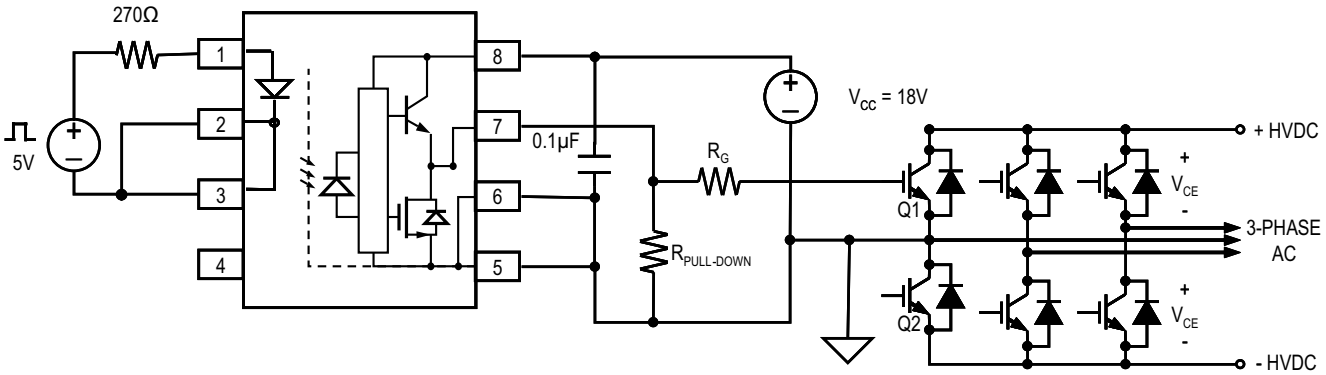
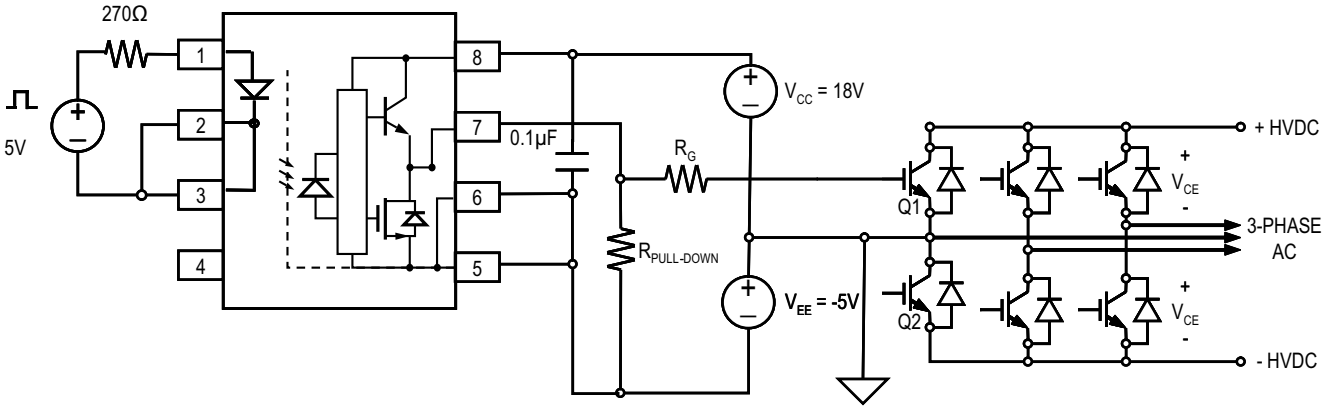


Figure 26 ACPL-H312/K312 Typical Application Circuit with Negative IGBT Gate Drive



Thermal Model for ACPL-H312/K312 Stretched-SO8 Package Optocoupler

Definitions:

R_{11}: Junction to Ambient Thermal Resistance of LED due to heating of LED.

R_{12}: Junction to Ambient Thermal Resistance of LED due to heating of Detector (Output IC).

R_{21}: Junction to Ambient Thermal Resistance of Detector (Output IC) due to heating of LED.

R_{22}: Junction to Ambient Thermal Resistance of Detector (Output IC) due to heating of Detector (Output IC).

P_1: Power dissipation of LED (W).

P_2: Power dissipation of Detector/Output IC (W).

T_1: Junction temperature of LED (°C).

T_2: Junction temperature of Detector (°C).

T_A: Ambient temperature.

ΔT_1: Temperature diff erence between LED junction and ambient (°C).

ΔT_2: Temperature deference between Detector junction and ambient.

Ambient Temperature: Junction to ambientthermal resistances were measured approximately 1.25 cm above optocoupler at ~23°C in still air.

Description

This thermal model assumes that an 8-pin single-channel plastic package optocoupler is soldered into a 7.62 cm × 7.62 cm printed circuit board (PCB). The temperature at the LED and Detector junctions of the optocoupler can be calculated using the equations below.

$$T_1 = (R_{11} \times P_1 + R_{12} \times P_2) + T_A \quad (1)$$

$$T_2 = (R_{21} \times P_1 + R_{22} \times P_2) + T_A \quad (2)$$

JEDEC Specifications	R_{11}	R_{12}, R_{21}	R_{22}
High K board	311	111	168

NOTE Maximum junction temperature for above parts: 125°C.

Quick Gate Drive Design Example Using ACPL-H312/K312

The total power dissipation (PT) is equal to the sum of the LED input-side power (PI) and detector output-side power (PO) dissipation:

$PT = PI + PO$

$PI = I_{F(ON),max} \times V_{F,max}$

where,

$I_{F(ON),max}$ = 16 mA (Recommended Operating Conditions)

$V_{F,max}$ = 1.8V (Electrical Specifications (DC))

$PO = PO(BIAS) + PO(SWTICH) = I_{CC2} \times (V_{CC2} - V_{EE}) + \Delta V_{GE} \times Q_G \times f_{SWITCH}$

where,

PO(BIAS) = Steady-state power dissipation in the driver due to biasing the device.

PO(SWITCH) = Power dissipation in the driver due to charging and discharging of power device gate capacitances.

I_{CC2} = Supply Current to power internal circuity = 3.0 mA (Electrical Specifications (DC))

$\Delta V_{GE} = V_{CC2} + |V_{EE}| = 18 - (-5V) = 23V$ (Application example)

Q_G = Total gate charge of the IGBT or MOSFET as described in the manufacturer specifi cation = 24 0nC (approximation of 100A IGBT which can be obtained from IGBT data sheet)

f_{SWITCH} = switching frequency of application = 10 kHz

Similarly using the maximum supply current I_{CC2} = 3.0 mA.

$PI = 16\ mA \times 1.8V = 28.8\ mW$

$PO = PO(BIAS) + PO(SWITCH)$

$= 3.0\ mA \times (18\ V - (-5\ V)) + (18V + 5V) \times 240nC \times 10\ kHz$

$= 69\ mW + 55.2\ mW$

$= 124.2\ mW$

Using the given thermal resistances and thermal model formula in this data sheet, we can calculate the junction temperature for both LED and the output detector. Both junction temperatures should be within the absolute maximum rating. For this application example, we set the ambient temperature as 78°C and use the high conductivity thermal resistances.

LED junction temperature,

$T_1 = (R_{11} \times P_1 + R_{12} \times P_2) + T_A$

$= (311 \times 28.8 + 111 \times 124.2) + 78$

$= 22.7 + 78 = 100.7°C$

Output IC junction temperature,

$T_2 = (R_{21} \times P_1 + R_{22} \times P_2) + T_A$

$= (111 \times 28.8 + 168 \times 124.2) + 78$

$= 24 + 78 = 102°C$

TIn this example, both temperature are within the maximum 125°C. If the junction temperature is higher than the maximum junction temperature rating, the desired specification must be derated accordingly.

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